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BANK 0 OPERATING VOLTAGE = 3.3V

PROGRAMMABLE CLOCK GENERATOR

Place Close to U2
ZYNQ BANK 500

**ZYNQ CONFIG MODE SELECT**

- **VMODE** 1 — MIO Bank 1 Voltage = 1.8V
- **VMODE** 0 — MIO Bank 0 Voltage = 3.3V

**Boot Modes**

- **BOOT_MODE[4]**
  - 1: PLL Bypassed
  - 0: PLL Used

- **BOOT_MODE[3]**
  - 1: Independant JTAG
  - 0: Cascaded JTAG

- **BOOT_MODE[2]**

- **BOOT_MODE[1]**

- **BOOT_MODE[0]**

<table>
<thead>
<tr>
<th><strong>BOOT_MODE[0]</strong></th>
<th><strong>BOOT_MODE[1]</strong></th>
<th><strong>BOOT_MODE[2]</strong></th>
<th><strong>BOOT_MODE[3]</strong></th>
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**Limit the Stub length to less than 10mm**

**MicroSD Card**

**QUAD SPI FLASH**

**UART HEADER**

**PS MIO**

- MIO7
- MIO6
- MIO5
- MIO4
- MIO3
- MIO2
- MIO1
- MIO0

**QSPI IOs**

- QSPI_CLK
- QSPI_0
- QSPI_1
- QSPI_2
- QSPI_3

**SDIO QSPI**

- SD_CLK
- SD_DAT0
- SD_DAT1
- SD_DAT2
- SD_DAT3
- SD_DETECT

**PS CLK**

- PS_CLK33M2

**VCCO MIO**

- VCCO_MIO0_1
- VCCO_MIO0_2

**PS POR**

- PS_POR_L6
- PS_POR_BC7

**USER LEADS**

- USER_LEAD 17

**JTAG**

- JTAG_BOOT_EN 17
DISABLED INTERNAL REGULATORS

100 Ohm Differential

PHY provides integrated Termination

PHYAD[0] = 0
VDDO_LEVEL = 1.8V for 88E1318

HW CONFIG SETTING:

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<th>CONFIG Value Assignment</th>
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<tbody>
<tr>
<td>0</td>
</tr>
<tr>
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For Lab Test Only

CONFIG

ETH_TXD[3:0]
ETH_TXCLK
ETH_TXCTL
ETH_RXD[3:0]
ETH_RXCTL
ETH_MDIO
BOARD_RESET_L6,17
...
Enable 100-ohm internal termination on all LVDS inputs
populate R95 & remove R96 to bypass RESET circuit