Practical Parallella expansion board design

My path to an autonomous SDR device

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Outline

About the speaker

- Linux and free software "geek" since 1999
- M.Sc. in C.S. + some E.E.
- General orientation towards low level
  - Embedded, Kernel, Drivers and such.
  - Hardware (Digital stuff, FPGA or RF)
- Interest in various telecom and SDR projects for several years
  - Osmocom
  - GNURadio
  - In my spare time
- Kickstarter backer
  - And got the various evolutions (Proto / Rev0 / Rev1 / Rev 1.1)
  - Thanks Andreas !

Application

What to do with my Parallella ?

- Autonomous SDR device
  - Record / Analyze / Generate RF signals on-the-go
- Requirements
  - DSP intensive $\Rightarrow$ computational power
  - Battery operation
  - Portable
- Peripherals
  - LCD
  - Touch screen
  - RFIC
  - Battery control
  - Audio (?)
  - Low Speed control (SPI/I2C/GPIOs/LEDs/Buttons)
  - Knob (All test instruments needs Knobs !)

Application
Why it's a great fit

- Computational power
  - FPGA: Simple high-throughput DSP
  - Epiphany: Balanced throughput/complexity DSP
  - ARM: Control / Higher protocol stack levels
- Low Power
  - Needed for battery operation
- GPIOs !
  - 48 GPIOs
  - High-Speed differential connector
  - Flexible V_{IO}

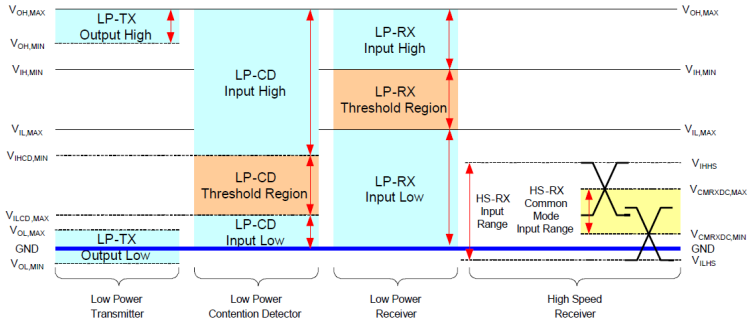
Application
Limitations

- "Only" 48 GPIOs available
  - $\Rightarrow$ Use them wisely
- Unique V_{IO}
  - $\Rightarrow$ May require level shift
- No MGTs
  - No JESD204B (ADC/DAC serial link)
  - No SATA
  - No eDP
- eLINK bandwidth
  - Fixed now ?

LCD
Interface selection

- 3 main types of interface
- Parallel
  - Simple
  - High pin count
  - Not so popular with recent high resolution panels
- eDP
  - Very fast serial link (multi Gb/s)
  - Zynq HR IOBs can't go that fast
  - Would need MGTs, not available on Parallella
- MIPI-DSI
  - Fast serial link (hundreds of Mb/s)
  - Not directly drivable from ZYNQ
  - But with some low complexity external help, it's doable

LCD
MIPI DSI Phy

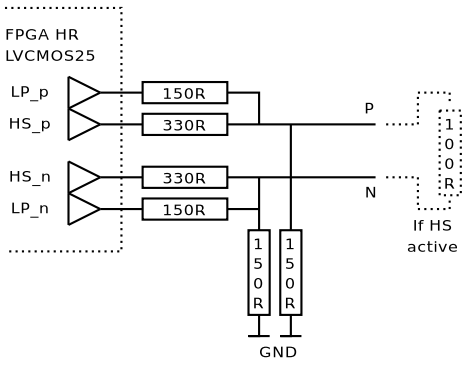


- N data lanes + 1 clock lane
- 1 lane = P + N signals
- LP mode: 1.2V signalling, 50 ohm driver impedance
- HS mode: Differential signalling into 100 ohm, 200mV CM, 200mV swing

LCD
MIPI DSI Phy v1

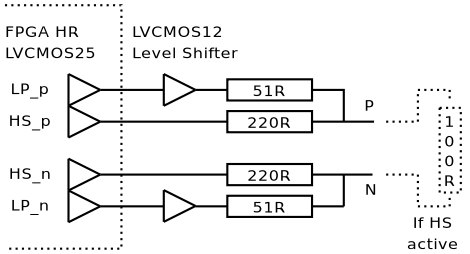
- Pros:
  - Simple & Cheap
- Cons:
  - For 4 lanes MIPI-DSI, uses 20 FPGA GPIOs
  - In IDLE LP11 state, burns 8.5 mA per signal

	LP driver	HS driver
LP0	0	*HiZ*
LP1	1	*HiZ*
HS0	0	0
HS1	0	1



LCD
MIPI DSI Phy v2

- Add LVCMOS 1.2v level shifter to drive LP branch
- Pros:
  - Still Simple & Cheap
  - LP11 is now low-power
  - Can share lane 2,3,4 LP signals from FPGA
  - Could also get rid of clock LP signals
  - For 4 lanes MIPI-DSI, usage down to 14 FPGA GPIOs
- Cons:
  - Adds an active component

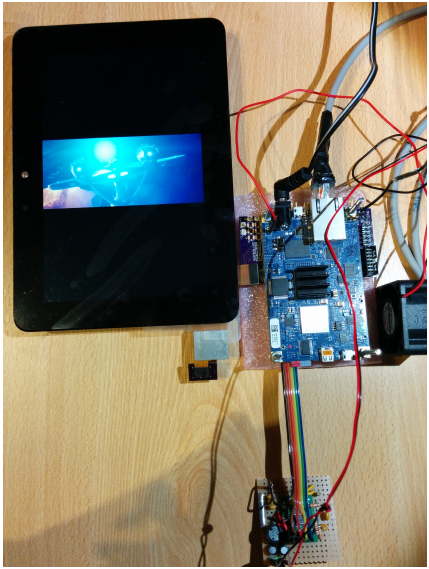


LCD
Selection

- Kindle Fire HD 7 inch
- Available as LCD+Digitizer assy from ebay for 60 USD
- LCD
  - Model `LD070WX3`
  - 800 by 1280 resolution
  - MIPI-DSI 4 lane interface
  - Datasheet available
  - Connector known and somewhat available
  - Kindle bootloader (u-boot) GPL with MIPI init sequence
- Digitizer
  - Integrated Atmel mXT768E controller
  - No datasheet
  - **but** there is a GPL kernel driver
  - Unknown connector

LCD

It works

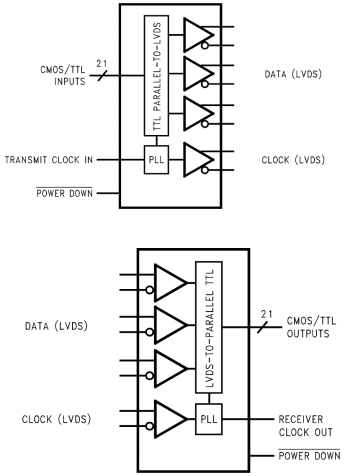


SDR
RFIC: LMS6002D

- Use the Myriad RF module
  - At least at first
  - Avoid dealing with weird package
  - Avoid dealing with RF part
- Available
  - Owned some already
  - Not the cheapest though
- Lots of open source resource available
  - Full docs open
  - Driver / Control code from other projects

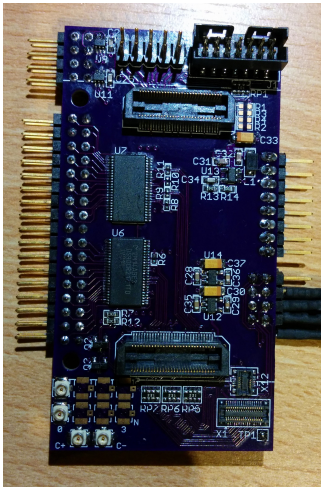
SDR
Interface

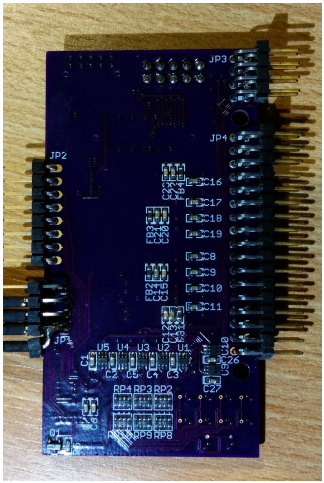
- Raw parallel data interface is 14 signals
  - RX and TX would use 28 GPIOs
  - Way too much !
- Use external LVDS SerDes chips
  - Selected "Channel Link" SerDes from TI
  - RX and TX now use 12 GPIOs (6 diff pairs)
  - Bonus: 2.5v / 3.3v level conversion to Myriad RF
- Some down sides
  - Costs money / space / power
  - On TX, recovered clock will be used for the ADC, watch for phase noise !
- Status
  - Prototype built last week
  - Didn't actually try it yet



Final words
Current State

- Display
  - PHY working
  - Work needed on HDL and Software side
- SDR
  - Begin testing





Thanks

Thank you for your attention !

Questions ?

Any questions ?